

AMENDMENTS TO THE CLAIMS

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of Claims:

Claims 1-3 (Canceled).

4. (Currently Amended) A method of forming a self-aligned buried contact pair, comprising:

[[a.]] depositing a lower ~~an oxide~~ layer on a substrate having diffusion regions;

[[b.]] forming a plurality of bit lines having bit line sidewall spacers on the lower oxide layer;

[[c.]] forming a ~~first~~ an upper interlayer dielectric (ILD) layer on the lower oxide layer, the plurality of bit lines and bit line sidewall spacers;

[[d.]] etching the ~~first~~ upper ILD layer and the lower oxide layer to expose a pair of adjacent diffusion regions in the substrate simultaneously;

[[e.]] forming a pair of buried contact pads on the exposed pair of adjacent diffusion regions in the substrate; and

[[f.]] forming a capacitor on each of the pair of buried contact pads.

5. (Currently Amended) The method as claimed in claim [[4]] 46, wherein the oxide layer is formed using a thermal oxidation process.

6. (Currently Amended) The method as claimed in claim 4, wherein the ~~first~~ upper ILD layer is deposited using a chemical vapor deposition (CVD) process.

7. (Currently Amended) The method as claimed in claim 6, further comprising: planarizing the ~~first~~ upper ILD layer after depositing the ~~first~~ upper ILD layer.

8. (Currently Amended) The method as claimed in claim 7, wherein the ~~first~~ upper ILD layer is planarized using a chemical mechanical polishing (CMP) process.

9. (Currently Amended) The method as claimed in claim 4, wherein forming the pair of buried contact pads comprises:

depositing a pad layer on the pair of exposed diffusion regions; and
planarizing the pad layer and the first upper ILD layer to expose the plurality of bit lines.

10. (Original) The method as claimed in claim 9, wherein the pad layer is deposited using a CVD process.

11. (Currently Amended) The method as claimed in claim 9, wherein the pad layer and the first upper ILD layer are planarized using a CMP process.

12-16 (Canceled).

17. (Currently Amended) ~~[[A]] The method as claimed in claim 35 of forming a self-aligned buried contact pair, further comprising:~~

~~a. depositing a first interlayer dielectric (ILD) layer on a substrate having diffusion regions;~~

~~b. forming a first direct contact pad pads and first buried contact pads in the lower first ILD layer, each one of the first direct contact pads and first buried contact pads being aligned over one of the diffusion region adjacent the pair of adjacent diffusion regions of the substrate; and~~

~~c. forming a second ILD layer on the first ILD layer, the direct contact pads and the first buried contact pads;~~

~~d. forming a second direct contact pad pads in the intermediate second ILD layer, each one of the second direct contact pads being aligned over one of the first direct contact pad pads;~~

~~e. forming a plurality of bit lines including bit line sidewall spacers on the second ILD layer;~~

- ~~—— f. —— forming a third ILD layer on the second ILD layer, the plurality of bit lines and bit line sidewall spacers;~~
- ~~—— g. —— etching the third ILD layer and the second ILD layer to expose a pair of adjacent first buried contact pads simultaneously;~~
- ~~—— h. —— forming second buried contact pads on the exposed pair of adjacent first buried contact pads; and~~
- ~~i. —— forming a capacitor on each of the second buried contact pads.~~

18. (Currently Amended) The method as claimed in claim 17, wherein the first lower ILD layer is formed by a CVD process.

19. (Currently Amended) The method as claimed in claim 17, wherein the second intermediate ILD layer is formed by a CVD process.

20. (Currently Amended) The method as claimed in claim 17, wherein the third upper ILD layer is formed by a CVD process.

21. (Currently Amended) The method as claimed in claim 17, wherein forming the first buried contact pads and first direct contact pads comprises:

- patterning the first lower ILD layer;
- etching the first lower ILD layer;
- depositing a first pad layer over the etched first lower ILD layer; and
- planarizing the first buried contact pads, the first direct contact pads, and the first lower ILD layer.

22. (Currently Amended) The method as claimed in claim 21, wherein planarizing the first buried contact pads, the first direct contact pads, and the first lower ILD layer is performed by a method selected from the group consisting of a CMP and an etch-back process.

23. (Currently Amended) The method as claimed in claim 17, wherein forming the second direct contact pads comprises:

etching the ~~second~~ intermediate ILD layer;
depositing a conductive layer over the etched ~~second~~ intermediate ILD layer; and
planarizing the conductive layer to expose the ~~second~~ intermediate ILD layer so that the
conductive layer material only remains in the etched portion of the ~~second~~ intermediate ILD
layer.

24. (Original) The method as claimed in claim 23, wherein the conductive layer is
deposited using a CVD process.

25. (Original) The method as claimed in claim 23, wherein the conductive layer is
planarized using a CMP process.

26. (Currently Amended) The method as claimed in claim 17, wherein each of the
plurality of bit lines comprises:

a bit line barrier metal formed on the ~~second~~ intermediate ILD layer;
a WSi layer formed on the bit line barrier metal; and
a bit line mask formed on the WSi layer.

27. (Currently Amended) The method as claimed in claim 17, further comprising:
planarizing the third ILD layer after depositing the ~~third~~ upper ILD layer.

28. (Currently Amended) The method as claimed in claim 27, wherein the ~~third~~
upper ILD layer is planarized using a CMP process.

29. (Currently Amended) The method as claimed in claim 17, wherein forming the
second buried contact pads comprises:

depositing a third pad layer on the exposed pair of adjacent first buried contact pads;
and

planarizing the third pad layer and the ~~third~~ upper ILD layer to expose the plurality of
bit lines.

30. (Original) The method as claimed in claim 29, wherein the third pad layer is deposited using a CVD process.

31. (Original) The method as claimed in claim 29, wherein the third pad layer is planarized using a CMP process.

32-34 (Canceled).

35. (Currently Amended) ~~[[A]] The method of forming a self-aligned buried contact pair, comprising: a. depositing a first as claimed in claim 4, wherein the lower layer is a lower interlayer dielectric (ILD[[]]) layer on a substrate having a pair of diffusion regions; further comprising:~~

~~[[b.]] forming the pair of buried contact pads includes forming a pair of first buried contact pads in the lower first ILD layer, each one of the pair of first buried contact pads being aligned over one of the pair of diffusion regions in the substrate;~~

~~[[c.]] forming a second an intermediate ILD layer on the lower first ILD layer and the first buried contact pads;~~

~~[[d.]] forming [[a]] the plurality of bit lines on the lower ILD layer includes forming the plurality of bit lines having bit line sidewall spacers on the second intermediate ILD layer;~~

~~[[e.]] forming a third an upper ILD layer on the second intermediate ILD layer, the plurality of bit lines and bit line sidewall spacers;~~

~~[[f.]] etching the third upper ILD layer and the second intermediate ILD layer to expose the pair of first buried contact pads simultaneously;~~

~~[[g.]] forming second buried contact pads on the exposed pair of adjacent first buried contact pads; and~~

~~[[h.]] forming [[a]] the capacitor includes forming the capacitor on each of the second buried contact pads.~~

36. (Currently Amended) The method as claimed in claim 35, wherein the lower first ILD layer is formed by a CVD process.

37. (Currently Amended) The method as claimed in claim 35, wherein the ~~second~~ intermediate ILD layer is formed by a CVD process.

38. (Currently Amended) The method as claimed in claim 35, wherein the ~~third~~ upper ILD layer is formed by a CVD process.

39. (Currently Amended) The method as claimed in claim 35, further comprising: planarizing the ~~third~~ upper ILD layer after depositing the ~~third~~ upper ILD layer.

40. (Currently Amended) The method as claimed in claim 39, wherein the ~~third~~ upper ILD layer is planarized using a CMP process.

41. (Currently Amended) The method as claimed in claim 35, wherein forming the first buried contact pads comprises:

 patterning the lower ~~first~~ ILD layer;
 etching the lower ~~first~~ ILD layer;
 depositing a first pad layer over the lower ~~first~~ ILD layer; and
 planarizing the first pad layer to expose the lower ~~first~~ ILD layer so that the first pad layer only remains in the etched portion of the lower ~~first~~ ILD layer.

42. (Original) The method as claimed in claim 41, wherein the first pad layer is planarized using a method selected from the group consisting of a CMP process and an etch-back process.

43. (Currently Amended) The method as claimed in claim 35, wherein forming the second ~~[[BC]]~~ buried contact pads comprises:

 depositing a second pad layer on the exposed pair of adjacent first buried contact pads;
and

 planarizing the second pad layer and the ~~third~~ upper ILD layer to expose the plurality of bit lines.

44. (Original) The method as claimed in claim 43, wherein the second pad layer is deposited using a CVD process.

45. (Original) The method as claimed in claim 43, wherein the second pad layer is planarized using a CMP process.

46. (New) The method as claimed in claim 4, wherein the lower layer is an oxide layer.